Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A method for operating an integrated memory [[unit]] with a reduced number of external terminal pins including a common external terminal pin and having a memory cell field, which comprises:

internally generating addresses with a counter of the integrated memory;

receiving addresses and access data from outside the integrated memory unit with the common external terminal pin;

before a memory access, partitioning the memory cell field into a plurality of memory areas;

for a memory access, selecting one of the memory areas by applying a memory area address;

during the memory access, internally generating addresses ~~with the memory unit by the counter of the integrated memory~~ for the access to memory cells of one of the memory areas; and

transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through [[a]] the common external terminal ~~connection~~ pin of the integrated memory [[unit]].

Claim 2 (original). The method according to claim 1, which further comprises transmitting, with an initialization command, one of

a number to be determined of the memory areas; and

a size of the memory areas.

Claim 3 (original). The method according to claim 1, which further comprises transmitting one of a number of the memory areas and a size of the memory areas, with an initialization command

Claim 4 (original). The method according to claim 1, which further comprises:

transmiting a start address for the memory access; and

beginning with the start address, generating addresses for the access to the memory cells of the one of the memory areas.

Claim 5 (original). The method according to claim 1, which further comprises transmitting an interrupt command for one of

an interruption and a termination of the memory access at a time defined by the interrupt command.

Claim 6 (original). The method according to claim 1, which further comprises:

applying a selection signal to the memory unit; and

transmitting at least two commands for the memory access by the application of the selection signal to the memory unit.

Claim 7 (original). The method according to claim 6, which further comprises transmitting a readout command and a write command through the selection signal.

Claim 8 (original). The method according to claim 6, which further comprises transmitting at least one of an initialization command, an interrupt command, and a masking signal through the selection signal.

Claim 9 (original). The method according to claim 7, which further comprises transmitting at least one of an initialization command, an interrupt command, and a masking signal through the selection signal.

Claim 10 (original). The method according to claim 1, which further comprises applying an activation signal to each of the memory units for an activation of the respective memory unit given an operation of a plurality of memory units at a common data bus.

Claim 11 (original). The method according to claim 10, which further comprises additionally utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 12 (original). The method according to claim 10, which further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 13 (original). The method according to claim 1, which further comprises:

operating memory units at a common data bus; and

applying an activation signal to each of the memory units for an activation of the respective one of the memory units.

Claim 14 (original). The method according to claim 13, which further comprises additionally utilizing the activation signal

as a timing signal for operation of the respective memory unit.

Claim 15 (original). The method according to claim 13, which further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 16 (original). The method according to claim 1, which further comprises executing the partitioning step, the selecting step, the internally generating step, and the transmitting step only in a test mode of the memory unit for testing a functionality of the memory unit.

Claim 17 (new). A method for operating an integrated memory with a reduced number of external terminal pins and having a memory cell field, which comprises:

providing an integrated memory with:

a counter internally generating addresses; and

a common external terminal pin for receiving addresses and access data from outside the integrated memory;

before a memory access, partitioning the memory cell field

into a plurality of memory areas;

for a memory access, selecting one of the memory areas by applying a memory area address;

during the memory access, internally generating addresses for the access to memory cells of one of the memory areas; and

transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through the common external terminal pin of the integrated memory.